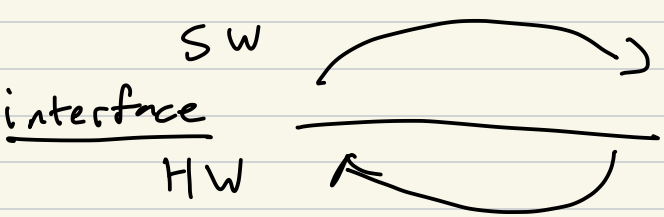
CS 315-01 Processor Components 2025-10-28

Project05 - incremental development

C coding
Data representation → IEEE 754 FP
Memory
RISC-V Assembly
RISC-V Machine Code
RISC-V Emulator
Cache Design
Digital Design
↓
Processor Design

Instruction Set Architecture (ISA)



Micro architecture
digital logic implementation

Computer Architecture

- Instruction set Architecture specification
  - machine code
  - registers
  - memory
  - assemblers
  - compilers
- Micro architecture
  - Digital Design
    - Schematic entry (visual)
    - HDL Hardware description Language
      - Verilog
      - IEEE VHDL

Moore's Law

The number of transistors doubles every 1.5 year for processors

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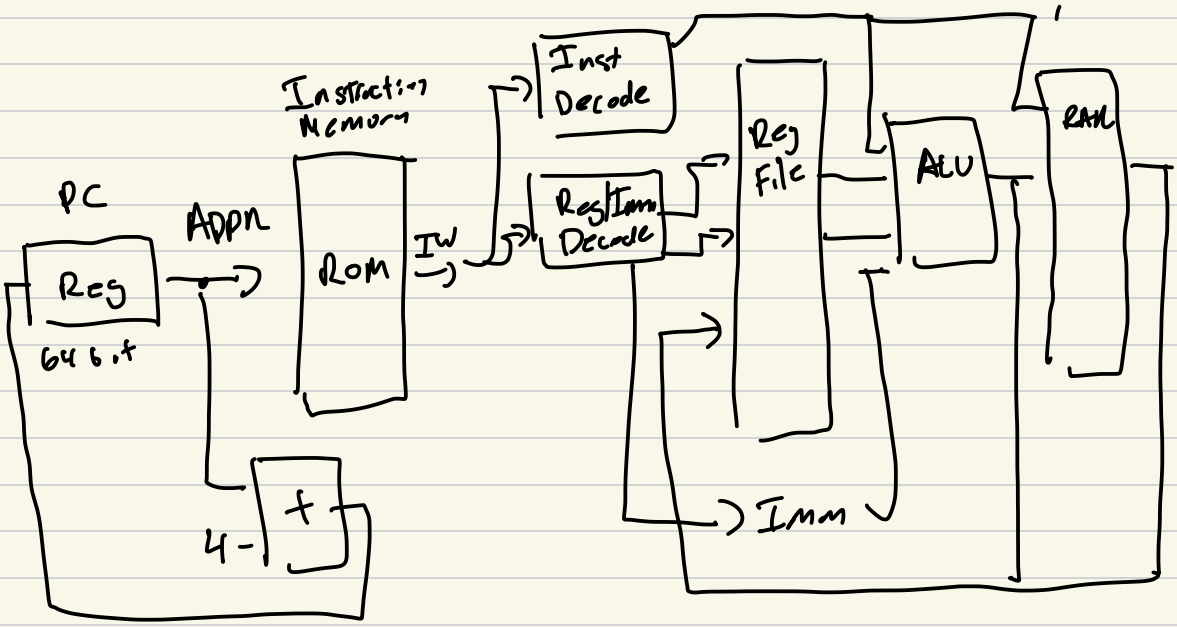
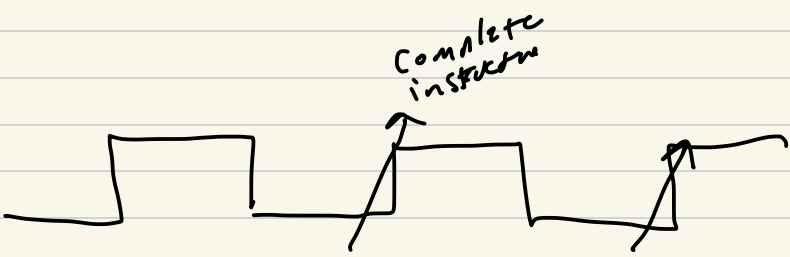
* Single-cycle processor
  [Multi-cycle processor]
* pipelined processor

Lab09 -> Lab10 -> Project06

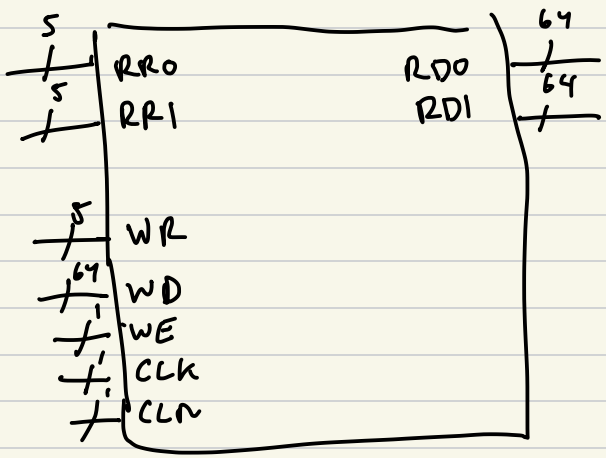
Single-Cycle Processor





Register File

- 32 64-bit registers: $x_0, x_1, \ldots, x_{31}$
- Read up to two register values in a single clock cycle.
- Write to a single register in a clock cycle
- x_0 (zero) will always be zero



RR read register

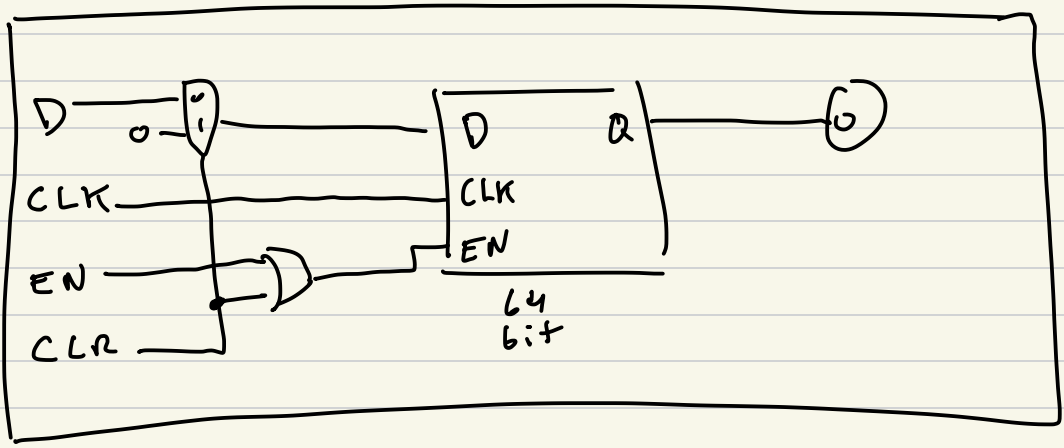
RD read data

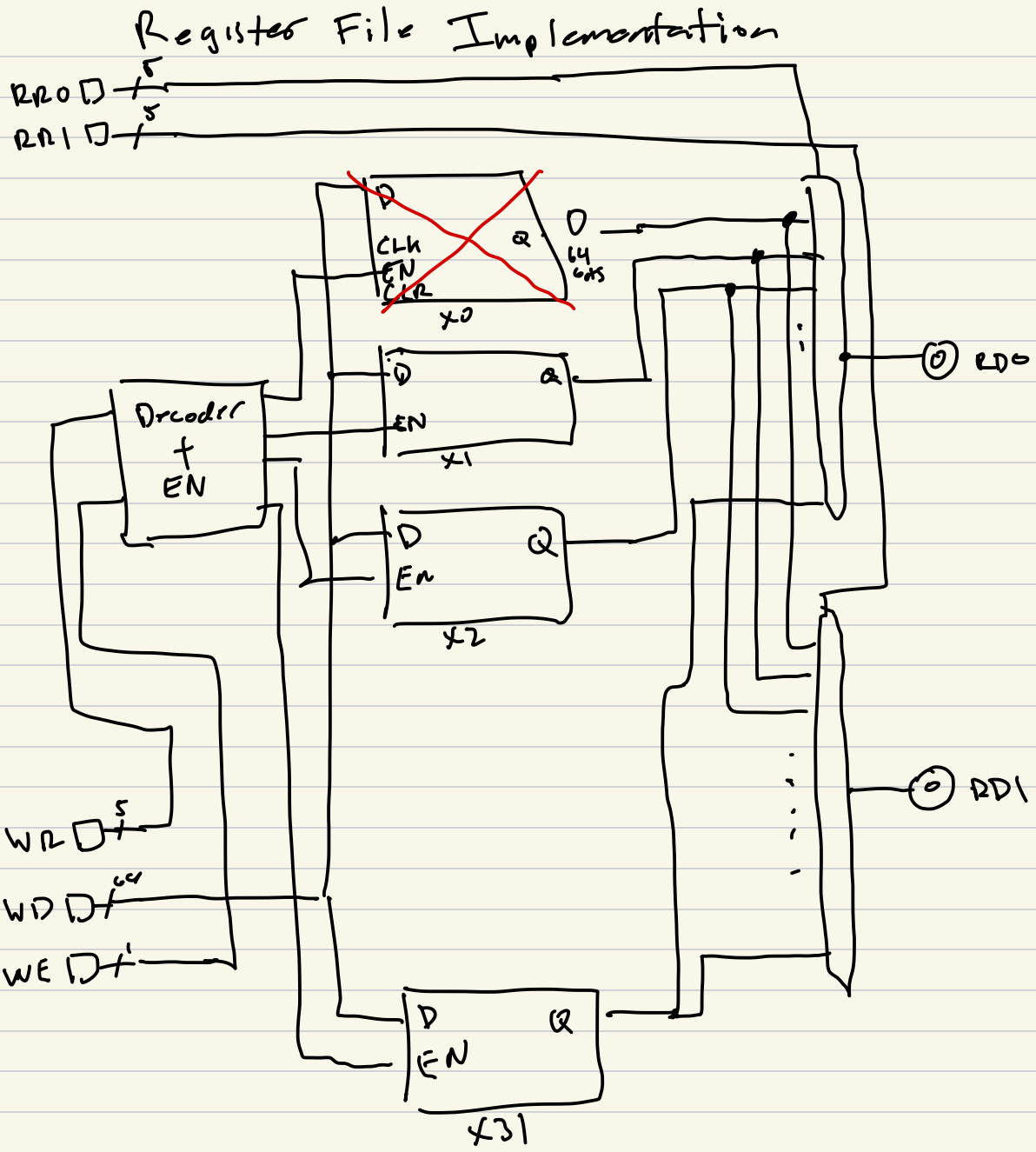
WR write register

WD write data

WE write enable

Adding CLR to the Digital Register




Register File Implementation
RR0
5
RR1
5
D
CLK
EN
CLR
Q
D
64
bits
x0
D
Q
EN
x1
Decoder
+
EN
D
Q
En
x2
RD0
RD1
WR
5
WD
64
WE
1
D
Q
EN
x31